Amendments to the Claims:

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

Claims 1-6 (canceled).

Claim 7 (previously presented): A method for secure access to at least one variable in a preemptively multitasking-controlled processor system, the method comprising the steps of:

providing a task scheduler for processing tasks;

providing an access status memory;

inputting, via an accessing task, a blocking information item into the access status memory before the secure access to the at least one variable;

checking, via the task scheduler and when there is a task change intended by the task scheduler during the secure access, the access status memory for an input blocking information item;

delaying the intended task change via the task scheduler when the blocking information item is input;

inputting a task change information item using the input blocking information item;

inputting, via the currently accessing task, a release information item into the access status memory at the end of the secure access; and

initiating the intended task change, via the currently accessing task, when the task change information item is input.

Claim 8 (previously presented): A method for secure access to at least one variable in a preemptively multitasking-controlled processor system as claimed in claim 7, the method further comprising the steps of:

activating a time monitoring system having a time period of at least a duration of the secure access; and

terminating the secure access after the expiration of the defined time period.

Claim 9 (previously presented): A method for secure access to at least one variable in a preemptively multitasking-controlled processor system as claimed in claim 8, the method further comprising the steps of:

checking contents of the access status memory at the end of the secure access and before the inputting of the release information item; and

deactivating the activated time monitoring system when the task change information item is present and transmitting a technical operating information item which initiates the intended task change to the task scheduler by the currently accessing task.

Claim 10 (previously presented): A method for secure access to at least one variable in a preemptively multitasking-controlled processor system as claimed in claim 7, the method further comprising the step of:

overwriting contents of the access status memory by the inputting of at least one of the blocking information item, the task change information item and the release information item into the access status memory.

Claim 11 (previously presented): A method for secure access to at least one variable in a preemptively multitasking-controlled processor system as claimed in claim 7, the method further comprising the step of:

forming the blocking information item, the task change information item and the release information item by at least one single-bit information item.

Claim 12 (previously presented): A method for secure access to at least one variable in a preemptively multitasking-controlled processor system as claimed in claim 7, the method further comprising the step of:

representing a variable by one of a variable of a software module which is stored in a memory unit and a hardware-related setting information item which is stored in a hardware register.